WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a sense amplifier group configured in hierarchy to read out data from a memory cell;

a complementary signal line group connecting a sense amplifier of a lower hierarchy level with a sense amplifier of a higher hierarchy level; and

a control circuit suppressing a drive of complementary signal lines by the sense amplifier of a lower hierarchy level connected to said complementary signal lines, and rendering active the sense amplifier of a higher hierarchy level connected to said complementary signal lines, before a potential difference between said complementary signal lines reaches a level of power supply voltage.

2. The semiconductor memory device according to claim 1, further comprising a write driver group configured in hierarchy to write data into a memory cell, wherein

a write driver of a lower hierarchy level and a write driver of a higher hierarchy level are connected by said complementary signal lines and a write designation signal line,

said write driver of a higher hierarchy level outputs write data and inverted data thereof to complementary signal lines of a lower hierarchy level connected to said write driver of a higher hierarchy level, and drives the write designation signal line of a lower hierarchy level connected to said write driver of a higher hierarchy level at a predetermined logic value, and

said write driver of a lower hierarchy level is rendered active when the write designation signal line of a higher hierarchy level connected to said write driver of a lower hierarchy level attains said predetermined logic value.

3. The semiconductor memory device according to claim 1, further comprising a write driver group configured in hierarchy to write data into a memory cell, wherein

a write driver of a lower hierarchy level and a write driver of a higher hierarchy level are connected by said complementary signal lines,

said write driver of a higher hierarchy level outputs write data to one signal line of complementary signal lines of a lower hierarchy level connected to said write driver of a higher hierarchy level, and drives the other signal line of said complementary signal lines of a lower hierarchy level at a predetermined potential in a range other than the range of change of said other signal line in a read mode, and

said write driver of a lower hierarchy level is rendered active when said other signal line attains said predetermined potential.

4. The semiconductor memory device according to claim 3, wherein

said write driver of a lower hierarchy level comprises a logical element connected to said other signal line,

said logical element providing an output of a first logic value when the potential of said other signal line is in the range of change in a read mode and provides an output of a second logic value when the potential of said other signal line is in a range other than said range.

5. The semiconductor memory device according to claim 1, wherein a predetermined sense amplifier in said sense amplifier group includes

a transmission gate provided between complementary signal lines of a higher hierarchy level and complementary signal lines of a lower hierarchy level,

said transmission gate being rendered conductive when in a data write mode.

6. The semiconductor memory device according to claim 1, wherein a predetermined sense amplifier in said sense amplifier group includes

a circuit to fetch a potential of complementary signal lines of a higher hierarchy level connected to said predetermined sense amplifier, and

an N channel MOS transistor provided between said circuit and complementary signal lines of a lower hierarchy level connected to said

predetermined sense amplifier,

said N channel MOS transistor being rendered conductive when in a data write mode.

7. The semiconductor memory device according to claim 1, wherein predetermined complementary signal lines are driven at an amplitude smaller than the amplitude of power supply voltage in a data write mode,

wherein a sense amplifier of a lower hierarchy level connected to said predetermined complementary signal lines, includes

an amplify circuit amplifying potentials of said predetermined complementary signal lines, and

a P channel MOS transistor provided between said amplify circuit and said predetermined complementary signal lines,

wherein, in a data write mode, said P channel MOS transistor is rendered conductive to have potentials of said predetermined complementary signal lines applied to said amplify circuit, and after said application, said P channel MOS transistor is rendered conductive, and said amplify circuit amplifies said applied potentials at a logic amplitude of power supply voltage, and complementary signal lines of a lower hierarchy level connected to said sense amplifier of a lower hierarchy level connected to said predetermined complementary signal lines are driven based on said amplified potentials.

8. The semiconductor memory device according to claim 1, wherein a predetermined sense amplifier in said sense amplifier group includes

an amplify circuit connected to complementary signal lines of a lower hierarchy level, and

a latch circuit connected to said amplify circuit and connected to complementary signal lines of a higher hierarchy level,

wherein said amplify circuit fetches potentials of said complementary signal lines of a lower hierarchy level at a timing based on a first clock to amplify said fetched potentials, and provide said amplified potentials to said latch circuit,

wherein said latch circuit drives said complementary signal lines of a higher hierarchy level at latched said amplified potentials at a timing based on a second clock different from said first clock.

9. The semiconductor memory device according to claim 8, wherein complementary signal lines of a higher hierarchy level connected to said predetermined sense amplifier are precharged at a timing based on said second clock, and

a sense amplifier of a higher hierarchy level than said predetermined sense amplifier is rendered active at a timing based on said second clock.